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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
REID, CHERYL M	

ART UNIT	PAPER NUMBER
2142	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/964,942	LOH ET AL.	
	Examiner	Art Unit	
	Cheryl M. Reid	2142	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 1, 11-13, 14-15, and 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dhir and further in view of Chiao.

Claim 1

- Dhir teaches of a data link circuit connectable to the Ethernet controller.....(Paragraph [0016]); a command and control link circuit (Paragraph [0014]); independent interface converter, receiving a clock signal from the clock generating system, said converter also receiving data from the data link circuit, converting a data stream and transmitting said converted data to the data link circuit; (Paragraphs [0006,0016]); Dhir is silent in regards to a clock generator system, receiving commands from the command and control link circuit and sending a first clock signal to the Ethernet controller, and a second clock signal to the circuit under test; and a mode select circuit, receiving a mode select signal from the command and control link circuit and sending an enable signal to a converter, wherein the clock generator system manipulates the clock signal to an

enabled converter to synchronize data transfer from the circuit under test to the Ethernet controller. Chiao teaches on these aspects. Chiao teaches of a clock generator system, receiving commands from the command and control link circuit and sending a first clock signal to the Ethernet controller, and a second clock signal to the circuit under test (Col 4, lines 15-39, Fig. 2); and a mode select circuit, receiving a mode select signal from the command and control link circuit and sending an enable signal to a converter (Col 15, lines 45-47), wherein the clock generator system manipulates the clock signal to an enabled converter to synchronize data transfer from the circuit under test to the Ethernet controller (Col 4, lines 6-8). Dhir's invention relates to programmable integrated circuits that can be used to handle different communication specifications (Paragraph [0001, 0014). Chiao's invention relates to computer bus interface adapters (Col 1, lines 20-35). Adding the above mentioned features to Dhir would accomplish his objective of developing an integrated circuit that can handle different communication specifications because the added features such as the multiplexer would allow various communication protocols to communicate with Dhir's system. It is for this reason that one of ordinary skill in the art at the time of invention would have been motivated to add the above mentioned features.

Claim 11

- Dhir teaches of connecting at least one independent interface converter to the circuit, to the Ethernet controller, and to a command and control center;

transmitting and receiving data among the circuit, the interface converter, and the Ethernet controller and wherein the data from the circuit is in a format selected from the group consisting of media independent interface (MII), serial media independent interface (SMII), and gigabit media independent interface (GMII). (Paragraph [0015]; Dhir is silent in regards to synchronizing the transmitting and receiving by adjusting clock signals to the circuit, the interface converter, and the Ethernet controller. Chiao teaches on this aspect (Col 4, lines 5-10). One of ordinary skill in the art at the time of invention would have been motivated to add the above mentioned features for the same reasoned discussed above in claim 1.

Claim 12 and 20

- Dhir teaches that the Ethernet controller receives and transmits data in an MII format (Paragraph [0015], lines 6-10).

Claim 13

- It was well known at the time of the art that synchronizing can be accomplished by using a fraction of a frequency of a master clock. This concept has been well known in the networking and digital logic arts for decades, and is commonly taught in introductory undergraduate digital logic courses.

Claim 14 and 18

- Dhir is silent in regards to synchronizing by stopping and starting said clock signals. Chiao teaches on this aspect (Col 2, lines 10-15, Col 3, lines 59-63). Adding the above- mentioned features to Dhir would result in a more accurate and efficient system. It is for this reason that one of ordinary skill in the art at the time of invention would have been motivated to add the above mentioned.

Claim 15 and 19

- Dhir is silent in regards selecting a mode, wherein selecting the mode also selects a format for an independent interface. Chiao teaches about selecting a mode (Col 15, lines 45-50). Chiao implicitly teaches that the mode also selects a format for an independent interface (Col 14, lines 30-35). One of ordinary skill in the art at the time of invention would have been motivated to add the above mentioned for the same reasons discussed in claim 14.

Claim 16

- Dhir teaches about connecting the circuit to an independent interface converter; transmitting and receiving data from the circuit and the converter; and controlling the circuit with an Ethernet LAN controller and synchronizing the circuit with the converter (Paragraph [0015]); Dhir is silent in regards to wherein the controller tests the circuit by synchronizing a speed of the Ethernet LAN controller with a speed of the circuit and wherein data from the device is in a format selected from the group consisting of a media independent interface (MII), a serial media

independent interface (SMII), and a gigabit media independent interface (GMII). Chiao teaches on these aspects (Col 3, lines 20-30, 59-63, Col 4, lines 7-8). One of ordinary skill in the art at the time of invention would have been motivated to add the above mentioned for the same reasons discussed in claim 1.

Claim 17

- Dhir is silent in regards to synchronizing occurring by furnishing a first clock signal to the Ethernet LAN controller, a second clock signal to the converter, and a third clock signal to the circuit. Chiao teaches about synchronizing and having a frist clock signal and a second clock signal (Col 4, lines 5-10, 15-35, Fig 2, Fig.6). Chiao is silent in regards to having a third clock signal. However, adding a third clock signal would have been obvious to one of ordinary skill in the art at the time of invention because it would result in a more efficient system. Adding the above mentioned features to Dhir's invention would result in a more efficient and reliable system. It is for this reason that one of ordinary skill in the art at the time of invention would have been motivated to make the above-mentioned modifications.

3. Claim 2 and 3-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dhir and Chiao as applied to claim 1 above, and further in view of Nam.

Claim 2

- Dhir teaches about converting data from one a first set to a second set (Paragraph [0006], lines 5-9). He is silent in regards to the at least one converter is selected from the group consisting of a first converter, a second converter and a third converter, the first converter converting a media independent interface (MII) data stream to a serial media independent interface (SMII) data stream and also converting an SMII data stream to an MII data stream, the second converter converting an MII data stream to a gigabit media independent interface (GMII) and also converting a GMII data stream to an MII stream, and the third converter converting an MII data stream to an MII data stream. Nam teaches about a multi-server system that include signal lines for MII, SMII, and GMII. Although, he did not explicitly teach about converting from one type of data (i.e. MII) to another type (i.e. SMII), he did implicitly teach that communications can occur between these signal lines (Paragraph [0014, 0059, 0068], Fig 8 and 10), this would require converting from one format to another. Dhir's invention relates to programmable integrated circuits that can be used to handle different communication specifications (Paragraph [0001, 0014). Chiao's invention relates to computer bus interface adapters (Col 1, lines 20-35). Nam's invention relates to combining multi-server systems into a single integrated box (Paragraph [0012]. One of ordinary skill in the art at the time of invention would have been motivated to add the above mentioned features for the same reasoned discussed above in claim 1.

Claim 3

- Both Dhir and Chiao are silent in regards to a first MII connector connected to the data link circuit, and a second connector connected to the data link circuit, said second connector selected from the group consisting of an MII connector, a GMII connector, and an SMII connector. Nam teaches on this aspect. One of ordinary skill in the art at the time of invention would have been motivated to add the above mentioned features for the same reasoned discussed above in claim 1.

Claim 4

- Dhir is silent in regards to the command and control link circuit receives and transmits signals selected from the group consisting of a master clock signal, a system clock signal, a reset signal and a mode select signal. Chiao teaches of the command and control link circuit receives and transmits signals selected from the group consisting of a master clock signal (Col 4, lines 35-38), a system clock signal (Col 4, lines 20-25), and a mode select signal (Col 15, lines 45-50). Chiao is also silent in regards to a reset signal. Nam teaches on this aspect (Paragraph [0065]). Adding the above- mentioned features to Dhir would result in a more accurate and efficient system. It is for this reason that one of ordinary skill in the art at the time of invention would have been motivated to add the above mentioned.

Claim 5-7

- In regards to converting from one data stream to another, please refer to the discussion of Claim 2 above. It was well known at the time of the art that a clock can be altered with the use of a counter to get reduced increments of the clock frequency for a second clock signal. The combination of a clock with a counter has been well known in the networking and digital logic arts for decades, and is commonly taught in digital logic courses.

Claim 8-10

- Both Nam and Chiao are silent in regards to an SMII crossover cable connecting said first converter with the data link circuit; a GMII crossover cable connecting said second converter with the data link circuit; MII crossover cable connecting said third converter with the data link circuit. Nam teaches on these aspects (Paragraph [0059, 0074,0076, Fig.7,8, and 10). One of ordinary skill in the art at the time of invention would have been motivated to add the above mentioned features for the same reasoned discussed above in claim 2.

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cheryl M. Reid whose telephone number is 571 272 3903. The examiner can normally be reached on Mon- Fri (7-3:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Harvey can be reached on (571)272-3896. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cmr

JACK D. HARVEY
SUPERVISORY PATENT EXAMINER